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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,774	CHEN ET AL.	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. In particular, the term "partial bypass reorder buffer" is not a well known term in the art and the term alone would not lead one of ordinary skill in the art to ascertain what the invention pertains to.

2. ¶ 9 of the specification contains the phrase, "functions units." It is believed that this is meant to be "functional units." Since the claims contain numerous spelling and grammatical errors, it is believed that the specification contains the same. Since the application contains a lengthy disclosure, it is the responsibility of the applicant to correct any other informal mistakes within the disclosure.

Claim Objections

3. Claims 1-58 are objected to because of the following informalities: Line 11 of claim 1 states "functions units." The examiner believes this was meant to be "functional units." On line 12, "detain" should be "detained." Appropriate correction is required.

4. Claim 2 is objected to because of the following informalities: On line 4 of claim 2, "detain" should be "detained" and the "the" after detained should be omitted OR the "the" before detain should be omitted. Appropriate correction is required.

5. Claim 2 is objected to because of the following informalities: Claim 2 refers to "a" FIFO buffer. It is unclear whether this buffer is the same as the reorder buffer claimed in claim 1. Appropriate correction is required.

6. Claim 3 is grammatically incorrect. For the purposes of this office action the examiner has inserted the word "or" to presume what was meant by the applicant. Appropriate correction is required.

7. There are multiple similar and other issues worthy of objection throughout the claims. It is the responsibility of the applicant to correct these issues.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. As per claim 2:

Lines 9 and 10 of claim 2 state that an instruction is shifted from a non-bypassable location to another non-bypassable location. This is not congruent with claim 1.

11. As per claim 8:

Claim 8 states that data from retired instructions would be sent from the reorder buffer. Retired instructions would not be in the reorder buffer.

12. Line 12 of claim 17 contains the phrase "the plurality of functions units." There is lack of antecedent basis for this phrase.

13. There are multiple similar and other 112 2nd issues throughout the claims. It is the responsibility of the applicant to correct these issues.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1-3, 6-11, 14-20, 22, 23, 25-30, 32, 33, 35-40, 42, 46-50, 52 and 56-58 are rejected under 35 U.S.C. 102(b) as being anticipated by Hennessy.

16. As per claim 1:

Hennessy teaches a data processing system for executing a plurality of instructions having a prescribed program order, the data processing system comprising:

a register file including a plurality of registers to store data (Hennessy Figure 4.3);

a reorder buffer including N buffer locations of which M buffer locations are bypassable and N-M buffer locations are non-bypassable, wherein N and M are integers and N >M (Hennessy 242, ¶5; Figure 4.3; Figure 4.4 (The examiner has labeled paragraph numbers)) (Hennessy discloses a scoreboard that can be used in his DLX processor. The scoreboard has 0 bypassable entries since a scoreboard only tracks the progress and availability of data rather than passing it. In Hennessy, M = 0 and N =

~6 (There are 6 instruction entries in Figure 4.4). Zero and six are integers and 6 > 0 and therefore fulfills the limitation.); and

a plurality of functional units, each functional unit capable of executing instructions regardless of prescribed program order (Hennessy 242, ¶ 5; 243, ¶ 4) (OOOX means that the FXUs are capable of executing instructions regardless of program order), and

wherein the reorder buffer temporarily stores data corresponding to the plurality of instructions (Hennessy Figure 4.4) and, when data of one of the plurality of instructions to be executed by a corresponding one of the plurality of functional units is temporarily stored in one of the M bypassable buffer locations, the detained one of the bypassable M buffer locations is transferred to the corresponding one of the functional units in order to execute the instruction (Since in Hennessy M = 0, this limitation does not apply), and

wherein the register file also stores data corresponding to retired ones of plurality of instructions (Hennessy 243, ¶ 5).

17. As per claim 2:

The data processing system of claim 1, wherein the reorder buffer includes a first-in-first-out (FIFO) buffer having N buffer locations is transferred to the register file and detain the nth – 1 one of the N buffer locations is shifted to the nth buffer locations (Hennessy 195) (It is inherent that Hennessy's scoreboard is a FIFO buffer since instructions need to be retired in order to keep precise interrupts. Since Hennessy

states that imprecise interrupts are something to be avoided and the DLX processor supports precise interrupts, it is inherent that the scoreboard is FIFO.), and

wherein data of one of the plurality of instructions to be executed by a corresponding one of the plurality of functional units is temporarily stored in one of the N-M non-bypassable buffer locations (Hennessy Figure 4.4), the corresponding one of the plurality of functional units waits until the data of one of the plurality of instructions is shifted from the N-M non-bypassable buffer locations to the M non-bypassable buffer locations (Hennessy 243, ¶ 5) (This limitation is incomprehensible; however, Hennessy states that his scoreboard keeps track of when FXUs can execute instructions included within the scoreboard.).

18. As per claim 3:

The data processing system of claim 2, wherein the reorder buffer comprising control circuitry to transfer the data in one of the bypassable M buffer locations to one of the functional units (Since M=0, this limitation does not apply; however, Hennessy does have control circuitry to transfer data to the FXUs, Figure 4.3.) and to shift or detain the N buffer locations (Hennessy Figures 4.5 and 4.6; 243, ¶ 5) (From the figures, it can be seen that instructions in non-bypassable locations are detained throughout the pipeline. Though it is not shown explicitly, it can be inferred that instructions are shifted out once they are in condition for retirement since the majority of programs contain more than six instructions and Hennessy comments that all instructions go through the scoreboard.).

19. As per claim 6:

The data processing system of claim 1, wherein the register file includes a plurality of inputs to access data as operands to execute one of the plurality of instructions and includes a plurality of outputs to output the operands for one or more instructions in a same cycle (Hennessy Figure 4.3).

20. As per claim 7:

The data processing system of claim 1, wherein the register file includes one or more write ports to receive data for storage from the reorder buffer (Hennessy Figure 4.3).

21. As per claim 8:

The data processing system of claim 7, wherein the reorder buffer includes one or more output ports to send data from one or more retired instructions in the N buffer locations (Hennessy 243, ¶ 5; Figure 4.3).

22. As per claim 9:

Hennessy teaches a data processing system for executing a plurality of instructions having a prescribed program order, the data processing system comprising:

a register file means including a plurality of register means to store data;

a buffering means including N buffer locations of which M buffer locations are bypassable and N-M buffer locations are non-bypassable, wherein N and M are integers and N >M (Hennessy 242, ¶5; Figure 4.3; Figure 4.4) (Hennessy discloses a scoreboard that can be used in his DLX processor. The scoreboard has 0 bypassable entries since a scoreboard only tracks the progress and availability of data rather than

passing it. In Hennessy, M = 0 and N = ~6 (There are 6 instruction entries in Figure 4.4). Zero and six are integers and 6 > 0 and therefore fulfills the limitation.); and

a plurality of functional means, each functional means capable of executing instructions regardless of prescribed program order (Hennessy 242, ¶ 5; 243, ¶ 4) (OOOX means that the FXUs are capable of executing instructions regardless of program order), and

wherein the buffering means temporarily stores data corresponding to the plurality of instructions (Hennessy Figure 4.4) and, when data of one of the plurality of instructions to be executed by a corresponding one of the plurality of functional means is temporarily stored in one of the M bypassable buffer locations, the data in one of the bypassable M buffer locations is transferred to the corresponding one of the functional means in order to execute the instruction (Since in Hennessy M = 0, this limitation does not apply), and

wherein the register file means also stores data corresponding to retired ones of plurality of instructions (Hennessy 243, ¶ 5).

23. Claims 10, 11 and 14-16 contain the same limitations as claims 2, 3 and 6-8 and are rejected for the same reasons.

24. As per claim 17:

Hennessy teaches, in a processor for executing a plurality of instructions having prescribed program order, the processor comprising:

a register file including a plurality of registers to store instruction data (Hennessy Figure 4.3);

a reorder buffer including N buffer locations of which M buffer locations are bypassable and N-M buffer locations are non-bypassable, wherein N and M are integers and N >M (Hennessy 242, ¶5; Figure 4.3; Figure 4.4) (Hennessy discloses a scoreboard that can be used in his DLX processor. The scoreboard has 0 bypassable entries since a scoreboard only tracks the progress and availability of data rather than passing it. In Hennessy, M = 0 and N = ~6 (There are 6 instruction entries in Figure 4.4). Zero and six are integers and 6 > 0 and therefore fulfills the limitation.), wherein the reorder buffer temporarily stores data corresponding to the plurality of instructions (Hennessy Figure 4.4);

a plurality of execution units, each execution unit capable of executing instructions regardless of prescribed program order (Hennessy 242, ¶ 5; 243, ¶ 4) (OOOX means that the FXUs are capable of executing instructions regardless of program order), and

an issue logic to issue data from the register file to one of the N buffer locations and (Hennessy 242, ¶ 3; 243, ¶ 5), wherein when data of one of the plurality of instructions to be executed by a corresponding one of the plurality of functional units is temporarily stored in one of the M bypassable buffer locations, the issue logic transfers data stored or to be stored in one of the bypassable M buffer locations to the corresponding one of the execution units in order to execute the instruction (Since in Hennessy M = 0, this limitation does not apply).

25. As per claim 18:

The processor of claim 17, wherein the register file also stores data corresponding to retired ones of plurality of instructions (Hennessy 243, ¶ 5).

26. As per claim 19:

The processor of claim 18, wherein the reorder buffer includes control circuitry to transfer, as one of the plurality of instructions is retired, the data in the nth one of the N buffer locations to the register file (Hennessy Figure 4.3; 243, ¶5), to shift the detained nth-1 one of the N buffer locations to the nth one of the N buffer locations (Hennessy Figures 4.5 and 4.6; 243, ¶ 5) (From the figures, it can be seen that instructions in non-bypassable locations are detained throughout the pipeline. Though it is not shown explicitly, it can be inferred that instructions are shifted out once they are in condition for retirement since the majority of programs contain more than six instructions and Hennessy comments that all instructions go through the scoreboard. This will be done in a FIFO manner to keep precise interrupts.).

27. As per claim 20:

The processor of claim 19, wherein the control circuitry waits when data of one of the plurality of instructions to be executed by a corresponding one of the plurality of execution units is temporarily stored in one of the non-bypassable N-M buffer locations shifts into one of the bypassable M buffer locations before transferring the data in one of the bypassable M buffer locations to the corresponding one of the plurality of execution units (Hennessy 243, ¶ 5; Figure 4.3) (Since M=0 in Hennessy, the control circuitry sends data to the execution units when the operands are ready rather than when an entry is shifted to an M location).

28. As per claim 22:

The processor of claim 17, wherein control circuitry further includes retire circuitry to retire data for one or more instructions in the reorder buffer to the register file (Hennessy 243, ¶ 5).

29. As per claim 23:

The processor of claim 17, wherein control circuitry further includes data hazard detection circuitry that detects a data hazard condition in data (Hennessy 243, ¶ 5).

30. As per claim 25:

The processor of claim 17, wherein the issue logic issues data for one or more instruction to the reorder buffer (Hennessy 243, ¶ 3 and 5).

31. As per claim 26:

The processor of claim 17, wherein the processor is at least one of an embedded processor or a microprocessor (Hennessy 97) (The DLX architecture is a fictional architecture; however, it is based on other real architectures that were implemented in microprocessors).

32. As per claim 27:

Hennessy teaches, in a processor for executing a plurality of instructions having prescribed program order, the processor comprising:

a register file means including a plurality of registers to store instruction data (Hennessy Figure 4.3);

a buffering means including N buffer locations of which M buffer locations are bypassable and N-M buffer locations are non-bypassable, wherein N and M are integers

and N >M (Hennessy 242, ¶5; Figure 4.3; Figure 4.4) (Hennessy discloses a scoreboard that can be used in his DLX processor. The scoreboard has 0 bypassable entries since a scoreboard only tracks the progress and availability of data rather than passing it. In Hennessy, M = 0 and N = ~6 (There are 6 instruction entries in Figure 4.4). Zero and six are integers and 6 > 0 and therefore fulfills the limitation.), wherein the buffering means temporarily stores data corresponding to the plurality of instructions (Hennessy Figure 4.4);

a plurality of execution means, each execution means capable of executing instructions regardless of prescribed program order (Hennessy 242, ¶ 5; 243, ¶ 4) (OOOX means that the FXUs are capable of executing instructions regardless of program order), and

an issue logic means to issue data from the register file means to one of the N buffer locations and (Hennessy 242, ¶ 3; 243, ¶ 5), wherein when data of one of the plurality of instructions to be executed by a corresponding one of the plurality of execution means is temporarily stored in one of the M bypassable buffer locations, the issue logic means transfers data stored or to be stored in one of the bypassable M buffer locations to the corresponding one of the execution units in order to execute the instruction (Since in Hennessy M = 0, this limitation does not apply).

33. Claims 28-30, 32, 33, 35 and 36 recite the same limitations as claims 18-20, 22, 23, 25 and 26 and are rejected for the same reasons.

34. As per claim 37:

Hennessy teaches a reorder buffer for executing instructions out-of-order, comprising:

a first-in-first-out (FIFO) buffer having N buffer locations of which M buffer locations are bypassable and N-M buffer locations are non-bypassable, wherein N and M are integers and N >M (Hennessy 242, ¶5; Figure 4.3; Figure 4.4) (Hennessy discloses a scoreboard that can be used in his DLX processor. The scoreboard has 0 bypassable entries since a scoreboard only tracks the progress and availability of data rather than passing it. In Hennessy, M = 0 and N = ~6 (There are 6 instruction entries in Figure 4.4). Zero and six are integers and 6 > 0 and therefore fulfills the limitation.); and

wherein the FIFO buffer temporarily stores data corresponding to the plurality of instructions for execution (Hennessy Figure 4.4) and, when data of one of the plurality of instructions to be executed is temporarily stored in one of the M bypassable buffer locations, the data in one of the bypassable M buffer locations is transferred to an execution unit corresponding to the instruction to be executed (Since in Hennessy M = 0, this limitation does not apply).

35. As per claim 38:

The reorder buffer of claim 27, further comprising:

control circuitry to transfer the data in one of the bypassable M buffer locations to an execution unit corresponding to the instruction to be executed (Since M=0, this limitation does not apply; however, Hennessy does have control circuitry to transfer data to the FXUs, Figure 4.3.)

36. As per claim 39:

The reorder buffer of claim 38, where the control circuitry, as one of the plurality of instructions is retired, transfers the data in the nth one of the N buffer locations to a register file (Hennessy Figure 4.3; 243, ¶5) and shifts the data in the nth-1 one of the N buffer locations to the nth one of the N buffer locations (Hennessy Figures 4.5 and 4.6; 243, ¶ 5) (From the figures, it can be seen that instructions in non-bypassable locations are detained throughout the pipeline. Though it is not shown explicitly, it can be inferred that instructions are shifted out once they are in condition for retirement since the majority of programs contain more than six instructions since Hennessy comments that all instructions pass through the scoreboard. This will be done in a FIFO manner to keep precise interrupts.).

37. As per claim 40:

The reorder buffer of claim 39, wherein the control circuitry waits for the data to move from one of the non-bypassable N-M buffer locations into one of the bypassable M buffer locations before transferring the data (Hennessy 243, ¶ 5; Figure 4.3) (Since M=0 in Hennessy, the control circuitry sends data to the execution units when the operands are ready rather than when an entry is shifted to an M location).

38. As per claim 42:

The reorder buffer of claim 38, wherein the control circuitry further comprises:

a hazard detection circuitry to detect a hazard condition including a data dependency condition (Hennessy 243, ¶ 5).

39. As per claim 46:

The reorder buffer of claim 38, wherein the control circuitry further comprises retire logic circuitry to retire data for one or more instructions to a register file (Hennessy 243; ¶ 5).

40. As per claim 47:

Hennessy teaches a reorder buffer for executing instructions out-of-order, comprising:

a first-in-first-out (FIFO) buffer means having N buffer locations of which M buffer locations are bypassable and N-M buffer locations are non-bypassable, wherein N and M are integers and N >M (Hennessy 242, ¶5; Figure 4.3; Figure 4.4) (Hennessy discloses a scoreboard that can be used in his DLX processor. The scoreboard has 0 bypassable entries since a scoreboard only tracks the progress and availability of data rather than passing it. In Hennessy, M = 0 and N = ~6 (There are 6 instruction entries in Figure 4.4). Zero and six are integers and 6 > 0 and therefore fulfills the limitation.); and

wherein the FIFO buffer temporarily stores data corresponding to the plurality of instructions for execution (Hennessy Figure 4.4) and, when data of one of the plurality of instructions to be executed is temporarily stored in one of the bypassable M buffer locations, the data in one of the bypassable M buffer locations is transferred to an execution unit corresponding to the instruction to be executed (Since in Hennessy M = 0, this limitation does not apply).

41. Claims 48-50, 52 and 56 recite the same limitations as claims 38-40, 42 and 46 and are rejected for the same reasons.

42. As per claim 57:

In a reorder buffer having N buffer locations of which M buffer locations are bypassable and N-M buffer locations are non-bypassable, wherein N and M are integers and N > M (Hennessy 242, ¶5; Figure 4.3; Figure 4.4) (Hennessy discloses a scoreboard that can be used in his DLX processor. The scoreboard has 0 bypassable entries since a scoreboard only tracks the progress and availability of data rather than passing it. In Hennessy, M = 0 and N = ~6 (There are 6 instruction entries in Figure 4.4). Zero and six are integers and 6 > 0 and therefore fulfills the limitation.), a method comprising:

fetching one or more instructions (Hennessy 127);

decoding one or more instructions (Hennessy 127);

checking if a data hazard condition exists from one of the decoded instruction (Hennessy 243, ¶ 5);

if a data hazard condition exists, checking if data is available in one of the bypassable M buffer locations for executing one of the decoded instructions (Hennessy 243, ¶ 5) (Since M=0 in Hennessy, this limitation does not apply; however, Hennessy's scoreboard does check for available operands.); and

transferring the data if available in one of the bypassable M buffer locations to an execution unit for executing one of the decoded instructions (Hennessy 243, ¶ 5; Figure 4.3) (Since M=0 in Hennessy, this limitation does not apply; however, Hennessy's scoreboard does send data to the FXU when operand data is ready.).

43. As per claim 58:

The method of claim 57, wherein the data hazard condition is a data dependency condition (Hennessy 243, ¶ 5).

Claim Rejections - 35 USC § 103

44. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

45. Claims 4, 5, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy as applied to claims 1 and 9 above and in view of Deao et al. (US Patent 5,970,241).

46. Hennessy teaches claims 1 and 9 for the reasons stated above.

47. As per claims 4 and 12:

Hennessy does not teach an ALU in combination with a load/store unit sharing one or more components, which Deao et al. do (Deao et al.: column 8, lines 2-6).

The advantages of sharing FXU components are well known in the art including reduced die space and the ability to support more FXUs, which increases ILP. Therefore, it would have been obvious to one of ordinary skill in the pertinent art that combining Deao et al. to Hennessy would provide the benefits of reduced die space and increased ILP.

48. As per claims 5 and 13:

The data processing system of claim 4 (12), wherein one of the functional units is a second ALU unit and wherein both the first ALU unit and the second ALU unit can execute an ALU instruction, respectively, in same cycles (Hennessy 279) (Deao et al.: column 8, lines 2-6) (Because Deao teaches a VLIW it is inherent that both functional units can execute an ALU instruction in the same cycle. Although Deao et al. is a VLIW, this aspect is inconsequential when applied to the execution units because the concept of VLIW is in the decoding and issuing of instructions; it is transparent to the FXUs. Therefore, the same will remain true when applied to Hennessy because Hennessy can support his processor as being superscalar.).

49. Claims 21, 24, 31 and 34, 43-45, 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy as applied to claims 17, 23, 27, 33, 38, 42, 48 and 52 above and in view of Johnson.

50. Hennessy teaches claims 17, 23, 27, 33, 38, 42, 48 and 52 for the reasons stated above.

51. As per claims 21 and 31:

Hennessy does not teach the processor of claim 17 (27), wherein the control circuitry includes an execution matching circuitry that checks if a tag signal associated with an executed instruction by one of the plurality of execution units matches a tag field in one of the M buffer locations and allows a result of the executed instruction to be stored in a buffer location having a matching tag field.

In particular, Hennessy does not teach allowing a result of the executed instruction to be stored in a buffer location having a matching field because in Hennessy, M = 0.

Hennessy does teach a buffering system that does allow a result of the executed instruction to be stored in a buffer location having a matching field for reservation stations (Hennessy 252). However, one of ordinary skill in the pertinent art would have recognized that reservation stations using Tomasulo's algorithm do not support precise interrupts.

On the other hand, Tomasulo's algorithm supports hardware register renaming, which can prevent WAW and WAR hazards (Hennessy 257).

Therefore, Hennessy would have motivation for combining his scoreboard (which is a reorder buffer without bypassing) to support precise interrupts and his reservation stations which prevent WAW and WAR hazards.

Johnson does just this (Johnson Figure 9.2). Johnson's reorder buffer is just like Hennessy's scoreboard in that it merely keeps track of the location and status of a value rather that the value itself. As can be seen by Johnson's figure, matching circuitry is present for matching tags of the reorder buffer to a buffer location holding the result in the reservation station. This would remain true when applied to Hennessy. The reservation entries would become the M bypassable entries.

One of ordinary skill in the pertinent art would have recognized that applying reservation stations to Hennessy's scoreboard such as in Johnson would provide

Hennessy with the ability to keep precise interrupts while preventing WAW and WAR hazards.

52. As per claims 24 and 34:

Motivation to combine Johnson to Hennessy is provided above. In the case when Johnson is combined with Hennessy, the reservation stations become the M bypassable entries and Hennessy and Johnson teach the processor of claim 23 (33), wherein the control circuitry further includes bypass circuitry, wherein if a data hazard condition is detected, the bypass circuitry is capable of transferring data in one of the bypassable M buffer locations to the issue logic (Hennessy 252, ¶ 3).

53. As per claims 43 and 53:

Motivation to combine Johnson to Hennessy is provided above. In the case when Johnson is combined with Hennessy, the reservation stations become the M bypassable entries and Hennessy and Johnson teach the reorder buffer of claim 42 (52), wherein the control circuitry further comprises bypass circuitry to receive hazard condition information from the hazard detection circuitry and to transfer the data in one of the bypassable M buffer locations to an execution unit corresponding to the instruction to be executed (Hennessy 243, ¶ 5; 252, ¶ 3).

54. As per claims 44 and 54:

Motivation to combine Johnson to Hennessy is provided above. In the case when Johnson is combined with Hennessy, the reservation stations become the M bypassable entries and Hennessy and Johnson teach the reorder buffer of claim 38 (48), wherein the control circuitry further comprises execution match detection circuitry

that detects if a tag signal from the execution unit matches a tag field in one of the bypassable M buffer locations, wherein if a match exists the execution match detect circuitry allows the bypass circuitry to transfer the data (Hennessy 243, ¶ 5; 252, ¶ 3) (Johnson Figure 9.2).

55. As per claims 45 and 55:

Motivation to combine Johnson to Hennessy is provided above. In the case when Johnson is combined with Hennessy, the reservation stations become the M bypassable entries and Hennessy and Johnson teach the reorder buffer of claim 38 (48), wherein the control circuitry further comprises an entry mux circuitry to allocate entries in the N buffer locations of the reorder buffer for storing data (Johnson Figure 9.2).

56. Claims 41 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy as applied to claims 38 and 48 above and in view of Witt et al. (US Patent 6,279,101).

57. Hennessy does not teach a state machine to determine if the reorder buffer is full or empty and to control whether any of the N buffer locations receives data, which Witt et al. do (Witt et al.: column 18, lines 32-45).

Witt et al. comment that using the buffer full signal will be able to tell the instruction decoder when the reorder buffer is incapable of receiving any additional results and that using the buffer empty signal will be able to assist in handling serialization conditions.

One of ordinary skill in the pertinent art would have realized that applying Witt et al. to Hennessy would provide the advantages of being able to tell the instruction decoder when the reorder buffer is incapable of receiving any additional results and to assist in handling serialization conditions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 12-8.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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